Strong electroadhesion at low voltage enabled by nanoscale roughness

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Electroadhesion conventionally relies on kilovolt potentials to bridge macroscopic gaps in many practical applications. Here, we demonstrate that the governing length scale for strong electroadhesion is not the device-level separation but the nanoscale gap distribution imposed by surface roughness. By combining boundary-element rough-contact modeling with macroscopic friction measurements on oxidized silicon interfaces, we establish a quantitative framework that predicts adhesion pressures approaching 100 MPa at voltages below 30 V. Furthermore, we uncover a strong polarity-dependent asymmetry in adhesion and friction, which we attribute to charge trapping at grain boundaries. Our findings demonstrate that strong, low-voltage electroadhesion is viable and identify mechanisms through which undesired electroadhesion can be suppressed.

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I. INTRODUCTION

Electroadhesion plays a critical role in many practical applications, ranging from microelectromechanical systems [1] and precision positioning [2] in the semiconductor industry to haptic [3] and biomedical devices [4] and robotics [5,6]. Electrostatic chucks, for example, are widely employed in wafer handling [7], while electroadhesive grippers have emerged as promising tools for soft robotics [5,8].

While electroadhesion [9] at solid-solid interfaces [10–14] can in principle be understood from contact mechanics and the nanoscale gap distribution between surfaces with roughness [15], most practical implementations [16,17] rely on macroscopic gaps that are much larger than the surface roughness [18]. In these systems [5,6], the separation is well defined and independent of the details of contact mechanics, enabling robust electroadhesion that typically requires kilovolt potentials. While effective, this reliance on high voltages poses significant engineering challenges, including dielectric breakdown, energy dissipation, and safety concerns [7], whereas the resulting electroadhesion is limited to pressures of only tens of kilopascals [16,17]. In contrast, exploiting nanoscale gaps [19–21] offers the possibility of much stronger electroadhesion pressures at low voltage [22,23], but requires predictive control over the interfacial geometry, which has so far remained experimentally unexplored for multiasperity contacts. Existing models typically rely on statistical descriptions of roughness and assume symmetric electrostatic response [24], but have not been quantitatively tested against experiments that resolve the actual interfacial geometry.

In this article, we demonstrate that macroscopic electroadhesion is fundamentally governed by nanoscale gap distributions imposed by surface roughness, and provide the first quantitative experimental validation of this principle in a multiasperity contact. By combining contact-resolved boundary-element modeling with macroscopic friction measurements, we show that adhesion pressures approaching 100 MPa can be achieved at voltages below 30 V, in quantitative agreement with theory. Importantly, we uncover a pronounced polarity-dependent electroadhesion that is not captured by existing symmetric models, revealing a previously unrecognized role of charge trapping in controlling interfacial electrostatic forces.

II. EXPERIMENT

We measured silicon-on-silicon friction using a rheometer (DSR 502, Anton Paar) inside a dry chamber (RH = 0.8%), as shown in the inset in Fig. 1 (see more details in Sec. A of the Supplemental Material [25]). A cleaned 3-mm-diameter polysilicon ball (Goodfellow) was brought into contact with an as-received monocrystalline silicon wafer (University Wafer); both surfaces were covered with a native oxide layer. The externally applied normal load (F_{external}) was kept constant at 40 mN, corresponding to a Hertz contact radius of 8.5 μm. During sliding, both externally applied normal load and dynamic friction force (F_f) at the contact interface were simultaneously measured by the rheometer. The ratio of these two forces gives the friction coefficient $\mu = F_f/F_{\text{external}}$. It is important to note that the measured friction coefficient may be affected by the adhesive force at the contact interface, which adds to the externally applied normal load and is balanced by the elastic repulsive force (F_{elastic}) generated at the contact points. The sliding speed imposed by the rheometer was fixed at 0.1 μm/s for all the

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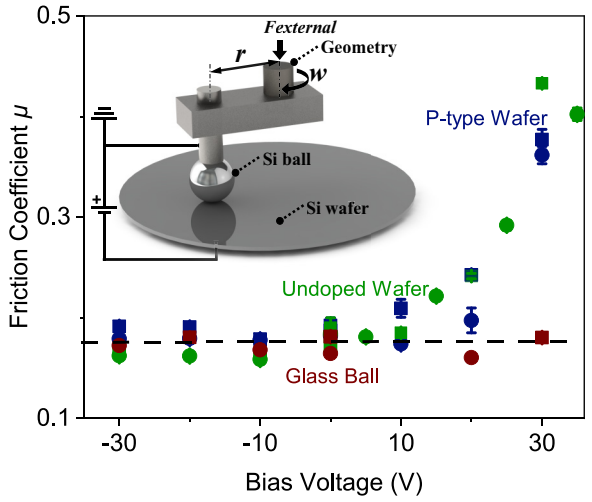

FIG. 1. Asymmetric dependence of friction coefficient (μ) on applied bias voltage (V). The blue, green, and dark red data correspond to the contacts of polysilicon ball-on-*P*-type wafer, polysilicon ball-on-undoped wafer, and glass ball-on-*P*-type wafer, respectively (see more experiments in Fig. S1 of the Supplemental Material [25]). To eliminate the influence of history-dependent effects (Fig. S2 in the Supplemental Material [25]), the applied bias voltage was first increased (solid squares) and then decreased (solid circles). The dashed line through the data points is drawn to guide the eye. Inset shows the experiential setup. A polysilicon ball, clamped inside a brass holder, slides on a silicon wafer inside a dry chamber. The holder, fixed at distance r from the axis of the rheometer's geometry, is driven at angular velocity ω, producing a sliding speed ωr at the contact.

measurements and the stable friction coefficient was reported after a few short sliding strokes. To investigate the dependence of friction on the applied bias voltage, the friction coefficient was measured while maintaining a target bias voltage (V) applied to the backside of the wafer, relative to the grounded polysilicon ball, using a power supply (Keysight E36232A). The applied bias voltage was varied between -30 and 30 V.

III. RESULTS AND DISCUSSION

As shown in Fig. 1, the dependence of the friction coefficient on the applied bias voltage at the silicon interfaces can be divided into two distinct regimes. In the positive bias voltage regime, the friction coefficient increases with increasing bias voltage. On the contrary, the friction coefficient remains unaffected under applied negative bias voltages.

It is well established that a potential difference across a dielectric layer—such as the air gap and native oxide present at our contact interfaces—generates an electric field that drives the accumulation of opposite charge carriers on the opposing surfaces. This, in turn, results in electroadhesion at the interface [26], effectively contributing an additional normal load and thereby increasing the friction force. In our case, by modeling the biased contact as a parallel-plate capacitor with a roughness-defined air gap, we predict an electroadhesion force on the order of mN at 30 V bias—sufficient to affect the friction force (see more details in Sec. B of the Supplemental Material [25]).

To refine the rough estimate of the electroadhesion force at a biased, deformed contact, we propose a simple adhesion model that quantitatively relates the electroadhesion force to the measured friction force. In this model, we attribute the interfacial adhesive force exclusively to the electroadhesion force generated in the noncontact (gap) area, where the local solid-air-solid gaps are treated as parallel capacitors. We also neglect the contributions from capillary adhesion as our dry experimental conditions suppress the formation of capillary bridges [27]. van der Waals interactions are not considered either, since the estimated van der Waals force is on the level of $\sim$100 μN based on the Derjaguin approximation with a function distance of 0.3 nm, insufficient to significantly affect the friction [28,29]. Consequently, the net force in the normal direction—the sum of the externally applied normal load ($\vec{F}_{\text{external}}$) and the electroadhesion force ($\vec{F}_{\text{ea}}$)—is balanced by the elastic repulsive force ($\vec{F}_{\text{elastic}}$) at the interface, as expressed by

$$\vec{F}_{\text{ea}} + \vec{F}_{\text{external}} + \vec{F}_{\text{elastic}} = 0. \tag{1}$$

We assume a constant proportion, μ_0, between the friction force and the net normal force, or elastic repulsive force, in accordance with the principles of load-controlled friction, as previously applied to similar silicon contact interfaces, $F_f = \mu_0 \times (F_{\text{ea}} + F_{\text{external}})$ [27,30,31]. This constant proportionality ratio can be extracted from the friction force measured at the contact interface in the absence of electroadhesion force, i.e., under zero bias voltage ($\mu_0 = F_f(V = 0)/F_{\text{external}}$). Therefore, we can calculate the net normal force, or the elastic repulsive force, F_{elastic}, as

$$|\vec{F}_{\text{elastic}}| = \frac{F_f}{\mu_0} = \frac{\mu(V) \times |\vec{F}_{\text{external}}|}{\mu_0}, \tag{2}$$

where $\mu(V)$ is the measured friction coefficient under an applied bias voltage V.

To obtain the contact deformation for electroadhesion force estimation, we conduct elastic contact calculations using the boundary element method (BEM) [25,32]). Unlike analytical models that rely on ensemble-averaged gap statistics [15,24,33], our BEM approach resolves the full spatial gap distribution [34]. Previous work has demonstrated that both BEM [35] and Persson-type [36] approaches yield consistent predictions of real contact area for similar interfaces, and that BEM-based contact solutions can quantitatively predict frictional behavior when the full gap distribution is resolved [27,29,31,37,38]. Using the elastic repulsive force from Eq. (2) as our calculation input, we obtain the three-dimensional nanoscale geometry of the deformed interface. The local electric field (E_i) is then calculated as $E_i = \frac{V}{u_i + h_0}$ [15,33] (Fig. S3 in the Supplemental Material [25]), where V, u_i, and h_0 are the applied bias voltage, the local interfacial gap, and the effective thickness of the dielectric layer, respectively. The parameter h_0 is determined by the thickness of the native oxide layer ($d = 2.2$ nm [39]) and the dielectric constant ($\kappa = 3.9$ [40]) of the native oxide layer, and is given by $h_0 = 2 \times d/\kappa$. Finally, the total electroadhesion force ($F_{\text{sim-ea}}$) is calculated as the sum of the locally experienced electroadhesion force ($F^i_{\text{sim-ea}}$) along the gap area within the contact

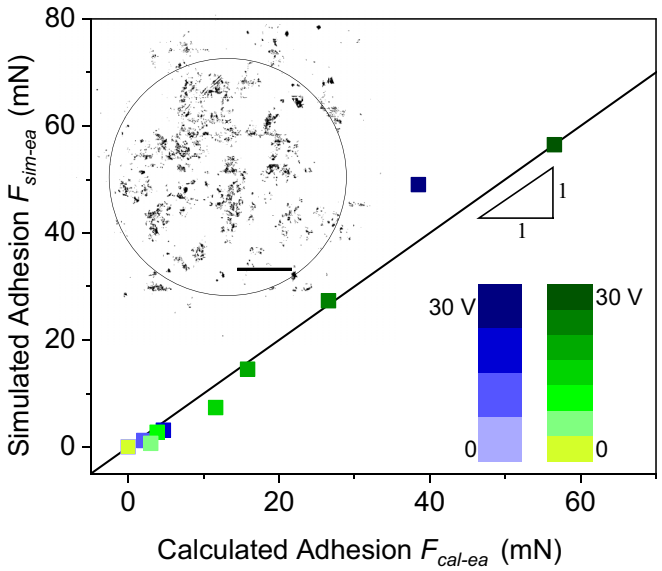

FIG. 2. Adhesion forces calculated from friction experiments and simulations. The blue and green data correspond to the contacts between the polysilicon ball and the *P*-type wafer, and the polysilicon ball and the undoped wafer, respectively. The corresponding color bar indicates the applied bias voltage for each case. The upper inset shows the calculated contact map at the interface between a wafer biased at +30 V and a grounded polysilicon ball, with the white and black regions corresponding to the solid-solid contact area and gap area, respectively. The black circle denotes the Hertzian contact area. Scale bar, 5 μm.

interface:

$$F_{\text{sim}-\text{ea}} = \sum F^i_{\text{sim}-\text{ea}} = \sum \frac{1}{2}\epsilon_0 E_i^2 A_i = \sum \frac{1}{2}\epsilon_0 \left(\frac{V}{u_i + h_0}\right)^2 A_i, \quad (3)$$

where A_i is the local gap area. Furthermore, the local interfacial capacitance C can be modeled as

$$C = \sum \frac{\varepsilon_0 A_i}{u_i + h_0}. \quad (4)$$

To verify our estimation of the electroadhesion force, we compare the simulated electroadhesion force ($F_{\text{sim}-\text{ea}}$) with the calculated electroadhesion force () from experiments. The latter is derived from the measured friction coefficient at the biased interface using Eqs. (1) and (2):

$$F_{\text{cal}-\text{ea}} = \frac{\mu(V) \times F_{\text{external}}}{\mu_0} - F_{\text{external}}. \quad (5)$$

As shown in Fig. 2, the electroadhesion forces obtained through the two methods show strong agreement, confirming the accuracy of our model and supporting our interpretation of the electroadhesion-enhanced friction in the positive bias voltage regime. This corresponds to a nominal adhesion pressure on the order of 100 MPa over the Hertzian contact area of ∼100 μm^2. We emphasize that the only adjustable parameter in our model is the native oxide thickness, fitted as 2.2 nm, a realistic value for silicon. Moreover, the constant friction coefficient observed at the biased wafer-on-grounded glass ball contact aligns with our model: The glass ball prevents charge carrier propagation to the interface, yielding an effective h_0 on the order of the ball diameter (∼mm), rather than the oxide thickness (∼nm). Consequently, the electric field ($E \propto 1/h_0$) becomes negligible, suppressing electroadhesion. Furthermore, our atomic force microscopy (AFM) adhesion measurements support the electroadhesion interpretation. The measured adhesion depends on the applied bias polarity, with a clear increase when electrons are driven toward the polysilicon surface, and a more complex response for opposite bias, consistent with polarity-dependent electroadhesion at a local Si-polysilicon contact (Fig. S4 and Sec. A in the Supplemental Material [25]).

The measured friction coefficient under negative bias voltage remains consistent with that observed at zero bias voltage (Fig. 1), indicating a negligible electroadhesion force. This contradicts with nonzero electroadhesion prediction based on Eq. (3). This discrepancy cannot be attributed to differences in wafer dopant types, as the biased friction shows similar response at the contact between an undoped silicon or an *N*-type wafer (Fig. S1 in the Supplemental Material [25]) and a grounded polysilicon ball. Tribocharging [41] appears negligible, given the stable friction force measured at zero bias voltage over the sliding distance. Furthermore, significant charge carrier depletion at the interface is unlikely due to the similar work functions of polycrystalline and monocrystalline silicon [42].

To explore the adhesion discrepancy between our model and experiments in the negative bias voltage regime, we repeated the bias friction measurements at the contact between two *P*-type wafers, instead of the original polysilicon ball-on-wafer configuration. We rotated the geometry (CP50-1/S, Anton Paar) to drive a glass pin mounted at its edge to slide the top grounded wafer (1 × 1 cm^2) over the biased substrate wafer at a constant velocity of 0.1 μm/s. The normal load was fixed at 23 mN by a dead weight. Meanwhile, the bias voltage was varied between −30 and 30 V, in intervals of 10 V. Before each change to the target voltage, the substrate wafer was grounded (0 V) until a steady friction force was achieved. The measured friction force, shown in Fig. 3, increases with increasing the applied bias voltage and exhibits a symmetric response for both positive and negative bias voltages of equal magnitude.

We therefore propose that the asymmetric adhesive response to opposite bias polarities (Fig. 1) results from the electronic properties of the polysilicon ball. Specifically, mobile positive charge carriers, i.e., holes, may encounter increased difficulty traversing bulk polysilicon compared with the mobile negative charge carriers. Charge traps within the bulk polysilicon may hinder a dense accumulation layer of positive charge carriers at the ball surface, which manifests as an increase in the effective dielectric thickness, h_0. This charge trap hypothesis is consistent with the history-dependent friction observed after bias removal at the grounded polysilicon ball-on-biased wafer contact (Fig. S2 in the Supplemental Material [25]): Under strong electric fields (Fig. S5 in the Supplemental Material [25]), charge carriers can get trapped at the silicon/oxide interface or within the oxide [43,44], delaying the decay of the electroadhesive interaction. While polysilicon displays history-dependent friction that lasts for minutes (Fig. S2 in the Supplemental

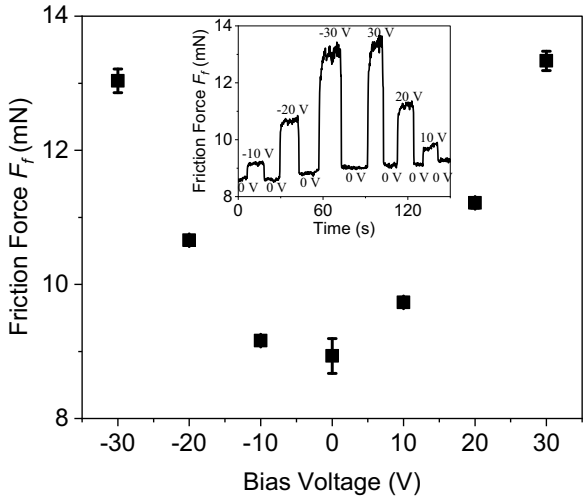

FIG. 3. Symmetric dependence of the measured friction force (F_f) on the bias voltage (V) applied on the substrate wafer at the wafer-on-wafer contact interface. The inset shows the real-time variation of friction force over applied bias voltage during the sliding.

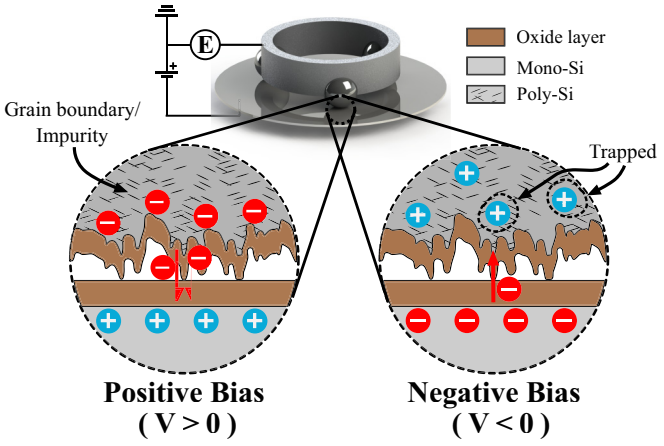

FIG. 4. Capacitance measurement setup and charge trapping mechanisms. The upper panel shows a schematic of the experimental setup. Three grounded polysilicon balls clamped by an aluminum ring are put on top of a dry thermally oxidized silicon wafer and charges transferred to the polysilicon balls during charging are measured using a Keithley 617 electrometer. Capacitance is calculated as the ratio of absolute charge change to the applied bias voltage. The bottom panel illustrates the polarity-dependent charge trapping mechanisms.

Material [25]), at the biased monocrystalline wafer-on-wafer interface such history-dependent friction is lacking (Fig. 3). Reported charge trap densities in polysilicon and oxide layers vary widely but can reach the level of $\sim 10^{13}\,\mathrm{cm}^{-2}$ (equivalent to $\sim 16\,\mathrm{mC/m}^2$) [40]. Although this is approximately an order of magnitude below our estimated surface charge density in the positively biased regime (Fig. S5 in the Supplemental Material [25]), volumetric traps in bulk polysilicon—especially at grain boundaries—can be sufficient to limit positive carrier transport over depths extending tens to hundreds of nanometers [45]. Moreover, the ideal parallel-plate assumption in our model provides an upper bound for the estimated charge density, as it relies on the idealized assumption of an infinite parallel-plate capacitor with a uniform, fixed surface charge distribution. In our model, the charge traps suggest that the voltage drop only partly takes place at the contact interface between a negatively biased wafer and a grounded polysilicon ball. Such small voltage drop only generates a weak electric field, resulting in minimal electroadhesion at the interfaces. When the polysilicon ball is replaced by a *P*-type wafer, the free mobility of positive and negative charge carriers within the bulk monocrystalline silicon wafer results in the same Coulombic interactions and thus electroadhesion force for both positive and negative bias voltages of equal magnitude.

To further support our interpretation, we directly measured the capacitance at the biased ball-on-wafer interface (see details in Sec. A of the Supplemental Material [25]). Notably, an electric current is observed across the biased contact interface [Fig. S6(a) in the Supplemental Material [25]], which scales linearly with the calculated elastic repulsive force (Fig. S7 in the Supplemental Material [25]). This proportionality further supports our load-controlled friction assumption, as the current is expected to scale with the real contact area [46], which is itself proportional to the elastic repulsive force [38]. To characterize the current-voltage behavior, we derived Fowler-Nordheim plots [Fig. S6(b) in the Supplemental Material [25]], from which tunneling energy barriers of approximately 1.05 and 1.69 eV were extracted for the *P*-type and undoped wafers, respectively, comparable to values reported for similar contact systems [47]. We exclude Joule heating as the origin of the observed friction increase. Control measurements on a sandblasted polysilicon ball (Fig. S8 in the Supplemental Material [25]) demonstrate that leakage currents can flow across the interface without inducing any corresponding friction enhancement in the positive bias regime, thereby experimentally decoupling heating from the friction increase. Nonetheless, our model remains valid even when such leakage current is ignored, as charge transfer through the contact interface does not eliminate the electroadhesion force generated among charge pairs in the gap regions.

To suppress charge leakage in capacitance measurements, we grow a 50 nm oxide layer on the wafer using dry thermal oxidation. Given the sensitivity of such small capacitance values ($\sim$pF estimated from Fig. S5 in the Supplemental Material [25]) to subtle fluctuations, we focus on the capacitance increase with increasing applied load, thereby isolating the capacitance contribution of the expanding contact area from all other sources of fluctuations. The measured capacitance increases by $14.83\% \pm 3.13\%$ under $+20$ V bias (from 7.90 ± 0.08 to 9.07 ± 0.23 pF), compared with $6.04\% \pm 1.84\%$ under -20 V bias (from 8.32 ± 0.05 to 8.82 ± 0.05 pF) as the load rises from 45 to 110 mN (Fig. S9 in the Supplemental Material [25]). This asymmetric increase is consistent with our charge carrier mobility hypothesis shown in Fig. 4: Positive charge carriers, i.e., holes, with reduced mobility in bulk polysilicon effectively increase the dielectric thickness, thereby lowering the interfacial capacitance between the negatively biased wafer and the grounded polysilicon ball.

Using Eq. (4), our measured capacitance ratio $\Delta C_-/\Delta C_+ \approx 0.43$ implies that the effective dielectric

thickness ($u_i + h_0$) under negative bias is larger by a factor of ∼2.3, indicating that charge transport limitations and trapping in the polysilicon lead to an effective increase in the dielectric thickness at the interface. Because the electroadhesion force scales inversely with the square of this separation, this increase alone leads to an approximately fivefold reduction in electroadhesion force. Furthermore, the electroadhesion force contributes to the total normal load, and thus also increases the elastic deformation of the contact, reducing the interfacial gap and further enhancing the electroadhesion [48,49]. This self-activation may amplify the sensitivity of adhesion and friction to the contrast in charge mobility between electrons and holes in the polysilicon. However, the present macroscopic experiments do not resolve the microscopic origin of charge trapping. A complete microscopic electroadhesion model will require further characterization of trapping-related properties, including grain structure, local electrostatic potential, and trap-state density.

IV. CONCLUSION

In conclusion, we establish that electroadhesion in macroscopic solid-solid contacts is governed by the nanoscale gap distribution imposed by surface roughness, rather than by the macroscopic separation typically assumed in device-level descriptions. By resolving the interfacial geometry through contact-resolved modeling and quantitatively validating it against experiments, we bridge the long-standing gap between theoretical predictions of roughness-controlled electroadhesion and its realization in multiasperity contacts.

This framework enables electroadhesion pressures approaching 100 MPa at voltages below 30 V, demonstrating that strong adhesion can be achieved in realistic interfaces without relying on large, externally defined gaps. Although the present experiments probe a Hertzian contact with a nominal area of approximately 100 μm^2, the governing principle is independent of contact size. Electroadhesion is determined by the nanoscale gap distribution within the real contact area rather than the nominal dimensions of the interface. The present framework therefore provides a route toward predicting and engineering electroadhesion in larger rough semiconductor interfaces, including electrostatic chucks, micro-electromechanical systems (MEMS) and precision-positioning systems, where the contact consists of many interacting microcontacts with similar nanoscale separations. Beyond surface roughness, tailoring the electronic properties of the contacting materials offers an additional route to enhance or suppress electroadhesion at low voltages. Importantly, we uncover a pronounced polarity-dependent electroadhesive response that directly contradicts the symmetric behavior assumed in existing models, revealing that charge transport and trapping can qualitatively modify interfacial electrostatic forces. Although the strong polarity dependence is observed here only in contacts involving polysilicon, the proposed mechanism is likely not unique to this material. It reflects a more general situation in which charge transport and trapping within one of the contacting solids modify the voltage drop across a rough interfacial gap. Materials with significant trap densities, such as polycrystalline or amorphous semiconductors, are therefore promising systems in which similar behavior may occur. Testing this hypothesis by systematically varying the grain structure of polysilicon or by investigating other trap-rich semiconductors represents an important direction for future work.

Adhesion controlled by nanoscale roughness is well known in wafer direct bonding, where roughness determines the equilibrium separation and bonding strength [19]. In contrast, the present work considers reversible electroadhesion under an externally applied voltage. By resolving the measured contact geometry and calculating the resulting electroadhesion stress, our framework extends rough-contact concepts to voltage-controlled adhesion in realistic semiconductor interfaces. The present framework may also provide a quantitative perspective on electrostatic contributions during bonding processes such as anodic bonding.

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DATA AVAILABILITY

The data that support the findings of this article are not publicly available. The data are available from the authors upon reasonable request.

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